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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,506	08/07/2003	Toshikazu Mizukoshi	OKI 361	8477

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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,506	MIZUKOSHI, TOSHIKAZU	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/18/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In response to the communication filed on April 12, 2005, claims 1 and 4-9 are active in this application.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 12, 2005 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 4-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Doi et al., U.S/6,187,648 B1.

Doi et al. teaches a method for forming a semiconductor device, which comprises a mask forming step comprised of sequentially forming a first insulating film 2 and a second insulating film 3 on a semiconductor substrate 1 (fig. 1a), followed by forming a mask for forming trenches on the second insulating film by patterning so as to expose a surface area of the second insulating

film corresponding to each trench formed on the semiconductor substrate (figs. 1a-1b, col. 3, lines 14-19); a trench forming step comprised of etching a portion extending from the surface area of the exposed second insulating film to an in-depth part of the semiconductor substrate using the mask for forming trenches (fig. 1b, inherently shows this method is applicable for forming a plurality of trenches), thereby forming the trenches on the semiconductor substrate; a depositing step comprised of removing the mask for forming trenches (figs. 1b), followed by depositing a third insulating film 5 by filling a third insulating film into each trench up to the height to cover the second insulating film (fig. 1c); a second oxide film 6 forming step performed through the third insulating film and after said depositing a third insulating film (figs. 1c-1d), and being comprised of subjecting the semiconductor substrate at a cornered portion of each trench to thermal oxidation, thereby forming a second oxide film (fig. 1d; col. 3, line 65 to col. 4, line 37), wherein said second oxide film forming step includes supplying oxygen from an upper side of the third insulating film so that the oxygen is diffused into the third insulating film, and so that an oxidative reaction starts at the cornered portion (i.e., oxygen is inherently provide from an upper side of the insulating film 5 since this is done through dry oxidation; accordingly, in order to form the oxide film 6, the oxygen must diffuse through the oxide film 5); a planarizing step performed after said second oxide film forming step (fig. 1d, see col. 4, lines 40-45 and the col. 2, lines 27-33), and comprising polishing and planarizing the third insulating film so as to expose the second insulating film (fig. 1d); and an element isolation portion forming step comprised of removing the second insulating film and the first insulating film, followed by etching the third insulating film such that a part of the third insulating film remains inside each trench, thereby

forming element isolating portion (fig. 1e, col. 4, lines 18-22 Note: a portion of the oxide layer 5 is also remove), see figs. 1a-2e and cols. 1-6 for more details.

Re claim 4, wherein the first insulating film is silicon oxide 2 (fig. 1a, col. 3, lines 7-8 and col. 6, lines 9-10) and the second insulating film is a silicon nitride film 3 (fig. 1a. col. 3, lines 9-13).

Re claims 5-6, wherein the third insulating film is a silicon oxide film 5 (fig. 1c and col. 6, lines 9-10).

Re claim 7-9, wherein the third insulating film is formed by HDP-CVD method (col. 3, lines 27-40).

Claims 1 and 4-6 are rejected under 35 U.S.C. 102(b) as anticipated by Ishitsuka et al., U.S./6,242,323 B1.

Ishitsuka et al. teaches a method for forming a semiconductor device, which comprises a mask forming step comprised of sequentially forming a first insulating film 2 and a second insulating film 3 on a semiconductor substrate 1 (fig. 51, also see examples 1-3), followed by forming a mask 43 (fig. 2C) for forming trenches on the second insulating film by patterning so as to expose a surface area of the second insulating film corresponding to each trench formed on the semiconductor substrate (fig. 2D); a trench forming step comprised of etching a portion extending from the surface area of the exposed second insulating film to an in-depth part of the semiconductor substrate using the mask for forming trenches 4a (fig. 51), thereby forming the trenches on the semiconductor substrate; a depositing step comprised of removing the mask for forming trenches (figs. 2E-2F), followed by depositing a third insulating film 4a by filling a third

insulating film into each trench up to the height to cover the second insulating film (fig. 53); a second oxide film 5 forming step performed through the third insulating film and after said depositing a third insulating film, and being comprised of subjecting the semiconductor substrate at a cornered portion of each trench to thermal oxidation, thereby forming a second oxide film (fig. 54), *wherein said second oxide film forming step includes supplying oxygen from an upper side of the third insulating film so that the oxygen is diffused into the third insulating film, and so that an oxidative reaction starts at the cornered portion (Ishitsuka et al. inherently shows this particular step because in order to form the oxide film 5 through thermal oxidation, oxygen must diffuse/pass through the insulating layer 4a in order to react with the substrate)*; a planarizing step performed after said second oxide film forming step, and comprising polishing and planarizing the third insulating film so as to expose the second insulating film (fig. 2H); and an element isolation portion forming step comprised of removing the second insulating film and the first insulating film, followed by etching the third insulating film such that a part of the third insulating film remains inside each trench, thereby forming element isolating portion 36 (fig. 2I, also see examples 1-3 for more details), see figs. 1A-70; cols. 1-40 for more details.

Re claim 4, wherein the first insulating film is silicon oxide 32 (fig. 2C) and the second insulating film is a silicon nitride film 42 (fig. 2C).

Re claims 5-6, wherein the third insulating film is a silicon oxide film 36 (fig. 2G).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishitsuka et al., U.S./6,242,323 B1 in view of Watanabe, U.S./6,417,073 B2.

Ishitsuka et al. disclosed above; however, Ishitsuka et al. is silent to using HDP-CVD method for forming silicon oxide.

Watanabe teaches a method for filling the trench with silicon oxide 311 (fig. 7A; col. 1, lines 40-45) by using HDP-CVD method.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use HDP-CVD silicon oxide as taught by Watanabe in the method of Ishitsuka et al. in order to provide good isolation, excellent uniformity, conformal step coverage, large wafer capacity and high throughput.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jack Chen
Primary Examiner
Art Unit 2813

April 18, 2005